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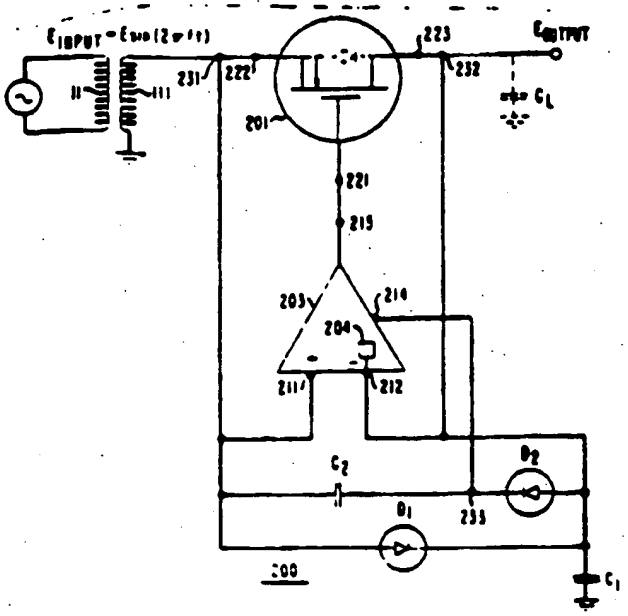

(57) Abstract

A two-terminal rectifier circuit (200), useful for converting an input a.c. voltage into an output d.c. voltage, is formed by a power MOSFET (201) which is controlled by a comparator (203) designed to turn on the MOSFET once during each a.c. cycle when the input a.c. voltage is nearly equal to its peak positive value thereby generating a relatively high d.c. output voltage.

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IMPROVEMENTS IN OR RELATING TO RECTIFIER CIRCUITS

Background of the Invention

This invention relates to rectifier circuits.

In the art of semiconductor electronics, very large scale integrated (VLSI) circuits typically require power sources of relatively small positive d.c. voltages, in the past typically about +5 volts. As the integrated circuit art progresses, even smaller d.c. voltages are becoming typical. In many situations, however, the only conveniently available power sources are a.c. voltage sources, typically having more than 5 volt peaks. For use by an integrated circuit requiring a power supply of 5 volts d.c., the a.c. voltage can be stepped down by a conventional transformer to about 5 volts peak a.c., and this 5 volt peak a.c. voltage must then be converted to 5 volts d.c. To this end, a semiconductor rectifier circuit can be used, typically a peak detector diode arrangement--that is, a pn junction diode feeding a capacitive load. One basic problem in such an arrangement arises from the forward junction diode voltage drop (about 0.7 volt or more in silicon) encountered in such a conventional peak detector diode arrangement. Thus, for an input a.c. voltage of peak E = 5.0 volts, the output voltage is less than about 4.3 volts, that is, in the range of about 0.7 volt to 1.0 volt or more below E for semiconductor junctions in silicon. As a consequence, undesirably large power losses result.

Summary of the Invention

According to this invention a rectifier circuit includes a power transistor device having a first high current carrying terminal serving as a rectifier circuit output terminal, a second high current carrying terminal serving as a rectifier input terminal, and a control terminal for turning the transistor device on and off, and a comparator having first and second input terminals connected to the rectifier circuit input and output

terminals respectively for supplying a control signal to the control terminal of the power transistor device to turn the device on when the voltage at the circuit input terminal exceeds the voltage at the circuit output terminal less a prescribed amount.

Description of the Drawings

FIG. 1 is a schematic circuit diagram of a prior art rectifier circuit arrangement;

FIG. 2 is a schematic circuit diagram of a rectifier circuit arrangement embodying the invention; and

FIG. 3 is a schematic circuit diagram of a rectifier circuit arrangement embodying the invention.

Detailed Description

A prior art approach, as illustrated in FIG. 1, taught in "Improving Power Supply Efficiency with MOSFET Synchronous Rectifiers," by R.S. Kagan et al, Proceedings of Powercon 9, Ninth International Solid-State Power Electronics Conference (July 1982), Session D, Paper D-4, pp. 1-5, at p. 4, Sections 6.1-6.3. Briefly, a full-wave rectifier circuit arrangement 10 includes a pair of power MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) 101 and 102, each hereinafter called a "power FET". Secondary transformer windings 111 and 121, energized by primary transformer winding 11, deliver a.c. input to the power FETs. Each power FET is inherently connected in parallel with its inherent unidirectional current inhibiting diode characteristic (indicated by dotted lines in FIG. 1), and each such power FET is connected in a conventional diode peak rectifier arrangement with respect to the input supplied to secondary transformer windings 111 and 121, respectively, and feeds output power to a resistive load (not shown) connected in parallel with a capacitive load C_L. To reduce the forward diode voltage drop, each power FET is turned on periodically by means of a sample (feed-forward) of the a.c. input delivered to the gate terminal of the FET. More specifically, the gate electrode of each power FET is fed input by an auxiliary

a.c. voltage developed by auxiliary secondary transformer windings 112 and 122, respectively. Thereby one of the power FETs (101) is turned on, and is maintained on, only in a time-neighborhood of the peak of the a.c. input cycle, i.e., only when the a.c input is at or near its peak (maximum) value; and the other of the power FETs (102) is turned on, and is maintained on, only in the neighborhood of each trough (minimum) of the a.c. cycle. In this way, the output voltage E_{OUTPUT} developed across an output load having a capacitive loading C_L desirably does not suffer from a full forward diode voltage drop. However, the gate-to-source voltage of the power FET thus varies as $(E_1-E_2)\sin(2\pi ft)$, where E_1 and E_2 are the peak voltages, respectively, delivered by the auxiliary transformer windings to the gate and source of the power FET, where f is the frequency of the a.c. input, and t is the time. Therefore, each turning on (and temporary remaining on) of the power FET at and near the peak of each a.c. cycle, when $\sin(2\pi ft)$ approaches its maximum value of unity, is not a sudden process, but is characterized by the relatively smooth and long transition characteristic of $(E_1-E_2)\sin(2\pi ft)$ when $\sin(2\pi ft)$ is approximately equal to ± 1. Accordingly, undesirably large amounts of energy are lost in the power FET during each a.c. cycle because of relatively large currents flowing therethrough (during the slow transitions) during time intervals when $\sin(2\pi ft)$ is very nearly equal to ± 1, i.e., intervals when the voltage drop across the FET is not negligible.

In another approach, taught by S. Waaben, in a paper entitled "FET Switching Devices for Powering of Telecommunications Circuits," published in Proceedings of Intelec 81, pp. 250-252, Third International Telecommunications Energy Conference (May 1981), a photoemitter (light-emitting diode) controlled the on-off condition of a photodetector which, in turn, controlled the on-off condition of a "power FET" arranged in a conventional peak rectifier arrangement, i.e., an

arrangement of the power FET (with its inherent unidirectional current inhibiting diode characteristic) feeding a capacitive output load. Specifically, the timing of the on-off condition of the photoemitter was arranged to control the timing of the power FET in a manner similar to the timing discussed above in connection with FIG. 1. Rectifier operation resulted in which voltage and power losses—otherwise caused by semiconductor diode junction forward voltage drops and by slow on-off transitions of the power FET—could be reduced substantially. However, the use of the optical control technology (photoemitters and photodetectors) means that the circuit was a three-terminal device including ground (one optical terminal and two electronic terminals) and entails obvious disadvantages in complexity and cost.

FIG. 2 shows a rectifier circuit arrangement 200 (half-wave portion) in accordance with this invention for delivering d.c. power to an output circuit terminal 232, including a transistor device 201. This transistor device 201 has one of its high current carrying terminals 222 connected to the rectifier circuit input terminal 231 and another of its high current carrying terminals 223 connected to the rectifier circuit output terminal 232. An a.c. input voltage $E_{INPUT}=E\sin(2\pi ft)$ is supplied at the circuit input terminal 231 by secondary transformer windings 111. The transistor 201 is advantageously a power transistor, that is, capable of handling power levels of the order of the power delivered to the circuit output terminal 232. This transistor 201 typically is a power FET having an inherent unidirectional current inhibiting diode characteristic indicated by the dotted line therein. A first unidirectional current inhibiting semiconductor junction diode D_1 can be added in parallel with the transistor 201 in case this transistor lacks sufficient forward current handling capacity when it is off. A first capacitor C_1 is connected between the first diode D_1 and ground but it should be understood that this first

capacitor C_1 can be omitted if the output capacitance C_L (shown in dotted lines) of the output load circuit (not shown) is sufficient to smooth out the voltage at the output terminal 232. Thus, the first diode D_1, in combination with the first capacitor C_1 (and/or the output capacitance C_L), forms a conventional peak detector and even in the absence of the transistor 201 would supply a d.c. voltage at the circuit output terminal 232; however, such a d.c. voltage as supplied by the peak detector is less than the peak E of the a.c. input by an undesirably large amount, that is, by the amount of the forward junction drop in the diode D_1. To reduce this undesirably large amount, the transistor device 201 is added together with control circuitry for controlling the voltage at the control terminal 221 thereof.

The on-off condition of the transistor 201 is controlled by output from the comparator 203 developed at the comparator's output terminal 215 and delivered to the control terminal 221 of the transistor 201. The comparator 203 has a positive input terminal 211 connected to the circuit input terminal 231 and a negative input terminal 212 connected to the circuit output terminal 232. The negative input terminal 212 is connected to a voltage level shifter 204 which down-shifts the voltage level of the negative input terminal 212 by a prescribed amount σ for comparison with the voltage level of the positive terminal 211. That is, the output of the comparator 203 at the comparator output terminal is relatively high when and only when the voltage at the positive input terminal 211 plus the prescribed amount σ exceeds the voltage E_{OUTPUT} at the negative input terminal 212. Thus, the output of the comparator shifts from low to high when $E\sin(2\pi ft)$ goes higher than $(E_{OUTPUT}-\sigma)$, or $E\sin(2\pi ft)+\sigma$ exceeds E_{OUTPUT}. A second junction diode D_2 and a second capacitor (C_2) are connected in series across the circuit input and output terminals 231 and 232, respectively. Power for the comparator 203 is supplied at the

comparator's power supply terminal 214 from a terminal 233 located between the second junction diode D_2 and the second capacitor C_2.

It should be noted that the diodes D_1 and D_2 together with the capacitors C_1 and C_2 form a voltage multiplier (doubler) ladder arrangement; the voltage at the multiplier's output terminal 233, and hence at the comparator's power supply terminal 214, relative to ground, is equal to $2E + E\sin(2\pi ft)$ less the sum of the forward diode voltage drops across D_1 and D_2, and hence, relative to the circuit input terminal 231, is equal to 2E less the sum of the forward diode voltage drops across D_1 and D_2.

During operation, the unidirectional diode characteristic (if any) inherent in the transistor device 201 plus the unidirectional diode characteristic of the first diode D_1, in combination with $C_1 + C_L$ in a diode peak detector arrangement, bring the output voltage E_{OUTPUT} at the circuit output terminal 232 to a steady d.c. voltage of E less a forward diode junction voltage drop (provided that $C_1 + C_L$ is sufficient), typically 5.0 volts less 0.7 volt or more, i.e., typically 4.3 volts or less. When the voltage of $E_{INPUT} = E\sin(2\pi ft)$ exceeds $E_{OUTPUT} - \sigma$, the transistor device 201 turns on and brings the output voltage E_{OUTPUT} to substantially $E-\sigma$. Hence, the transistor 201 turns on when $E\sin(2\pi ft)$ exceeds $E-2\sigma$. For example, if E = 5.0 volts and σ = 0.1 volt, then E_{OUTPUT} = 4.9 volts instead of the 4.3 volts or less resulting from the diode peak detecting arrangement alone. By adjusting σ, the output can be correspondingly adjusted. However, the value of σ is selected to be not too small, lest the time duration of the on condition of the power FET be too small for delivering sufficient charge to the output terminal, and not too large, lest the output voltage be undesirably too much lower than E.

Fig. 3 shows a specific embodiment of the

invention, particularly as to the details of a specific comparator. As shown in FIG. 3, a rectifier circuit arrangement 300 (half-wave portion) having a circuit input terminal 331 and a circuit output terminal 332, comprises a power FET 301 (T_1) with its source terminal 322 connected to the circuit input terminal 331, its drain terminal 323 connected to the circuit output terminal 332, and its gate terminal 321 connected to an output terminal 315 of a comparator 303. The power FET T1 has a threshold of about 2.5 volts and inherently has a unidirectional current inhibiting diode characteristic (indicated by dotted lines) which shunts the source terminal 322 to the drain terminal 323 of the power FET (T_1).

The purpose of the comparator 303 is to deliver feedback to the gate of the power FET to control its on-off condition suitably, as more fully described below. The comparator 303 has a power supply terminal for receiving power from an output terminal 333 of a voltage doubler arrangement. The voltage doubler comprises a pair of capacitors C_1 and C_2 connected in a ladder configuration to a pair of unidirectional current inhibiting diodes D_1 and D_2.

The comparator 303 includes a switching transistor T_2, local transistors T_3 and T_4, and resistors R_1 and R_2. The switching transistor T_2 is enhancement mode with a relatively sharp threshold of about 2.5 volts; and the transistors T_3 and T_4, connected as load devices (gate shorted to source), are depletion mode with source-drain currents in the saturation region (drain-source voltage above about 3 volts) of about 3 milliamps for zero gate voltages.

The capacitance of C_1 can be supplied by the output load capacitance C_L itself or by an added capacitor element such that the sum of C_1 and C_L is equal to the gate capacitance of the power FET multiplied by a factor of about 5 or more for advantageous performance. The capacitance of C_2 is advantageously

supplied by an added capacitor element having a capacitance of at least 5 times that of the gate capacitance of the power FET. The diode D_1 is in parallel with the inherent diode characteristic (dotted line) of the power FET. Thus, the diode D_1 is not necessarily present in the circuit 300 as a separate element but is ordinarily supplied by the inherent diode characteristic of the power FET. However, in case a power transistor lacking such a diode characteristic is used instead of the power FET, then an added diode element D_1 is advantageously to be added as a separate element.

It should be noted that the circuit output terminal is fed current both by the inherent diode of the power FET and the source-drain path power FET itself if and when it is on, as well as by the diode D_1. Thus, the voltage E_{OUTPUT} at the circuit output terminal 332 is maintained not only by the power FET but also by the diode D_1.

During operation, as more fully explained below, the transistor T_2 is off when and only when the instantaneous value of the a.c. voltage at the circuit input terminal 331 is at or near its peak, that is, when $E_{INPUT} = E\sin(2\pi ft)$ is equal to or in excess of $E_{OUTPUT}-\epsilon$, and the switching transistor T_2 is otherwise on. Thus, whenever the instantaneous value of the a.c. input voltage $E\sin(2\pi ft)$ at the circuit input terminal 331 is at or near its peak value and hence T_2 is off, then the voltage of the gate electrode terminal 321 of the power FET is driven by transistor load T_3 (acting as a current source) to the voltage of terminal 333, i.e., to the voltage 2E plus the voltage at circuit input terminal 331 less the relatively small voltage drop across D_2 and accordingly the power FET is then strongly on, since its gate voltage then exceeds its source voltage by almost 2E, i.e., almost about 10 volts (much more than the threshold of the power FET). On the other hand, whenever the a.c. input voltage is not at or near its peak value, the

switching transistor T_2 is on, as explained more fully below, and hence the gate voltage of the power FET is then clamped by T_2 to a value below threshold of the power FET, more specifically, essentially to the voltage at the circuit input terminal 331 and hence to the voltage at the source terminal 322 of the power FET 301. Thus the power FET is off when the a.c. input voltage is not at or near its peak. By "essentially" here is meant excluding the relatively small voltage drop across the resistor R_2 equal to the current through the load T_3 multiplied by R_2. For a resistance of R_2 equal to typically about 200 ohms or less, this voltage drop across R_2 is thus equal to about 0.6 volt or less, and this nonvanishing resistance reduces the voltage excursion of the gate of the power FET during each a.c. cycle and hence reduces the power loss in the gate circuit of the power FET. If such power loss is unimportant, R_2 can be made equal to zero. In any event, the drop across R_2 should be small enough to keep the power FET off when T_2 is on.

During operation, the switching transistor T_2 turns off (and hence the power FET T_1 turns on) at a time t_1 when the voltage at the gate of T_2 (and hence the voltage at terminal 316 of resistor R_1) attains a value which is equal to the instantaneous a c input voltage, $E_{INPUT} = E\sin(2\pi ft_1)$ plus a threshold voltage V_T of T_2, i.e., when the voltage at terminal 316 attains $E\sin(2\pi ft_1) + V_T$. On the other hand, the voltage at terminal 316 is equal to $E_{OUTPUT} + iR_1$, where i is the current supplied by the load T_4. Since the output voltage E_{OUTPUT} itself is equal to $E-\sigma$, it follows that the switching transistor T_2 turns off at a time t_1 when $E\sin(2\pi ft_1) + V_T = E - \sigma + iR_1$, i.e., at a time t_1 when:

$$E\sin(2\pi ft_1) = E - \sigma + iR_1 - V_T \qquad (1)$$

Likewise, as the a.c. input voltage subsequently

decreases from its peak E, the switching transistor T_2 turns on at a time t_2 when the a.c. input voltage falls (from the peak) to this same value of E_{INPUT}, i.e., at a subsequent time t_2 when $\sin(2\pi ft_2) = \sin(2\pi ft_1)$. Accordingly, E_{OUTPUT} will be substantially equal to $E-\sigma$ provided the capacitance $C_L + C_1$ is sufficient to maintain the voltage at the output terminal 332 at substantially this same value during the remainder of the a.c. cycle when T_2 is on and hence the power FET is off. Thus, setting $E\sin(2\pi ft_1)$ substantially equal to $E-2\sigma$ in Equation (1), it follows that iR_1 is equal to $(V_T-\sigma)$. In an illustrative case, the current i supplied by the load T_4 is equal to about 3 milliamps, and the threshold V_T of switching transistor T_2 is equal to about 2.5 volts, so that if R_1 is set equal to about 800 ohms, then σ is about 0.1 volt.

Accordingly, the comparator 303 acts as an ordinary comparator which delivers a high level output (a voltage equal to approximately 2E above the instantaneous a.c. input) when the input (E_{INPUT}) delivered to one of its input terminals (311) exceeds the input (E) delivered to another of its input terminals (312) less the prescribed amount σ, and which delivers a low level output (essentially equal to the instantaneous a.c. input) otherwise. In other words, the comparator 303 includes a level shifting property at its negative input terminal 312, to wit, a voltage level down-shift of σ. This down-shift property is thus incorporated in the comparator 203 of FIG. 2 as the voltage level shifter 204. In any event, this level shifter 204 should be selected to down-shift the voltage applied to the input terminal 212 of the comparator 203 by a (small) prescribed amount, such that the comparator 203 delivers its high level output at its output terminal 215 to the gate electrode terminal 221 of the power FET 201 when and only when the input voltage to the input terminal 211 of the comparator 203 exceeds the peak of the a.c. input voltage delivered at the circuit

input terminal 231 less the (small) prescribed amount σ. Typically the prescribed amount is about 0.1 volt for a 5 volt peak E of an a.c. input voltage applied at the circuit input terminal 231.

It should be noted that even though the approach of E_{INPUT} to its peak E is relatively slow in time because of its approach to a maximum, nevertheless the turning off of the switching transistor T_2, as E_{INPUT} reaches E less the (small) prescribed amount σ, is a well-defined sudden process. The suddenness of the process results from the well-defined threshold of transistor T_2. Thus the transistor T_2 advantageously has a relatively sharp threshold, that is, the source-drain impedance of T_2 has a relatively steep characteristic as plotted against its gate-to-source voltage.

It should be recognised that the rectifier circuit arrangements 200 and 300 are half-wave rectifiers and that, for full-wave rectification, and hence still smoother E_{OUTPUT}, a pair of each of such circuits should be connected in a conventional full-wave rectifier configuration.

Although the invention has been described in detail in terms of a specific embodiment, various modifications can be made.

For example, instead of the power FET, other switching transistors with suitable power handling capability and suitable threshold can be used. Moreover, instead of a voltage doubler (D_1, D_2, C_1, C_2), a voltage tripler or other source can be used. Finally, instead of a level down-shifter at the negative input terminal of the comparator, a level up-shifter at its positive input terminal can be used.

Claims

1. A rectifier circuit including a power transistor device (201) having a first high current carrying terminal (223) serving as a rectifier circuit output terminal, a second high current carrying terminal (222) serving as a rectifier circuit input terminal, and a control terminal for turning the transistor device on and off, and characterized by a comparator (203) having first and second input terminals (211, 212) connected to the rectifier circuit input and output terminals respectively for supplying a control signal to the control terminal of the power transistor device to turn the device on when the voltage at the circuit input terminal exceeds the voltage at the circuit output terminal less a prescribed amount.

2. A circuit as claimed in claim 1 characterized in that the comparator includes level shifting means (204) for shifting the voltage level applied to one of the comparator input terminals by the prescribed amount.

3. A circuit as claimed in claim 2 characterized in that the level shifting means serves to down-shift the voltage level applied to the second comparator input terminal.

4. A circuit as claimed in claim 2 characterized by a voltage multiplier (D_1, D_2, C_1, C_2) connected between the circuit input terminal and a power supply terminal (214) of the comparator.

5. A circuit as claimed in claim 4 characterized in that the multiplier includes a first capacitor (C_1), and first unidirectionally conductive means (D_1) connected between the circuit input terminal and a first terminal of the first capacitor.

6. A circuit as claimed in claim 5 characterized in that the first terminal of the first capacitor is connected to the circuit output terminal (232).

7. A circuit as claimed in claim 6 characterized by a second capacitor (C_2) connected between the circuit input terminal and the comparator power supply terminal.

and second unidirectionally conductive means (D_2) connected between the circuit output terminal and the comparator power supply terminal.

8. A circuit as claimed in any preceding claim characterized in that the transistor device is a power FET.

FIG. 1

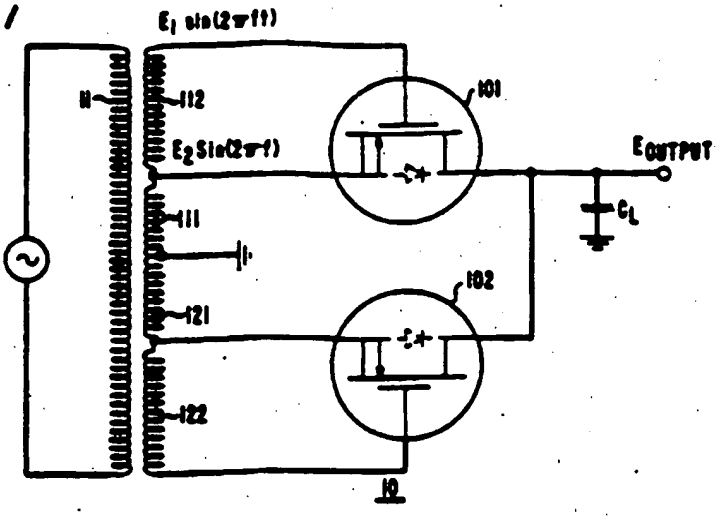
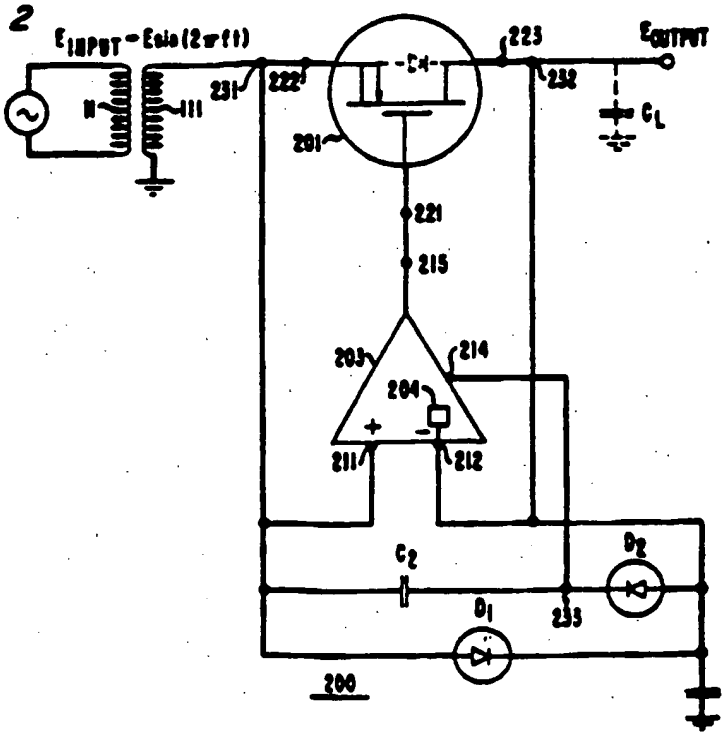


FIG. 2



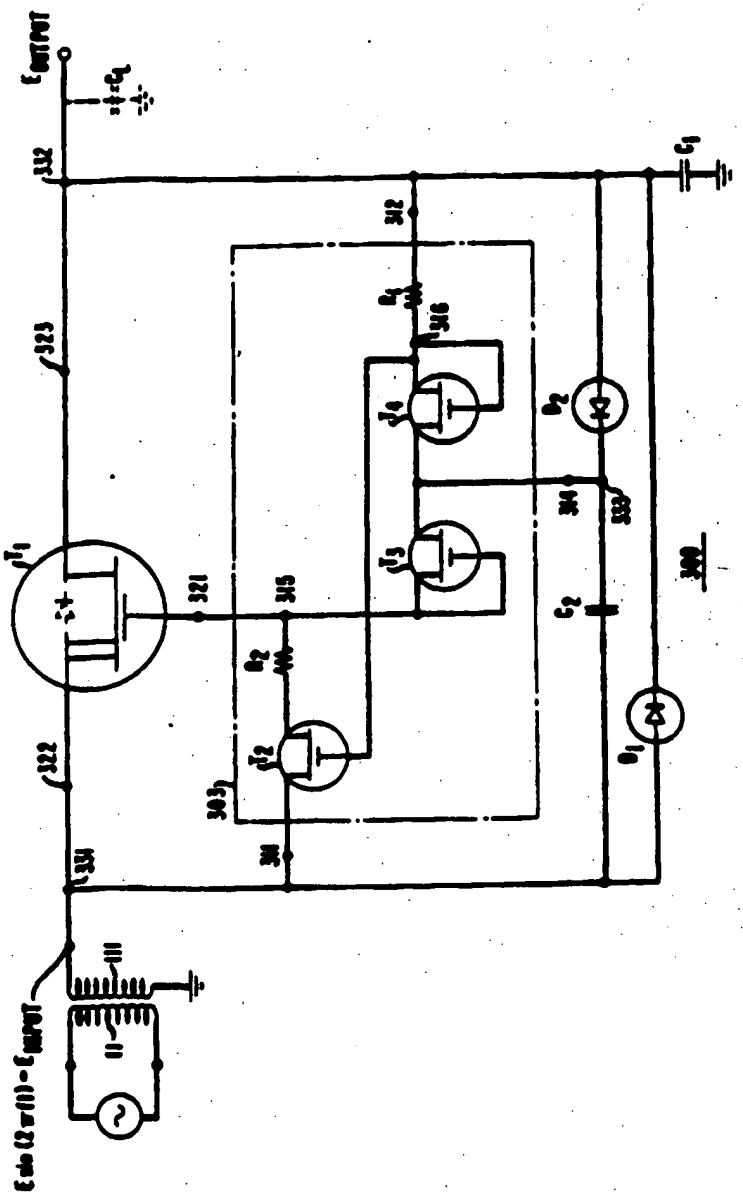


FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 84/01322

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4] : H 02 M 7/217; G 01 R 19/22

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC[4]	H 02 M; H 03 K; G 01 R

Documentation Searched other than Minimum Documentation to the extent that such Documents are included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category [15]	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	DE, A, 2801684 (H. FISCHER) 19 July 1979 see page 6, line 21 - page 7, line 7	1,8
A	US, A, 3354380 (S. FLY et al.) 21 November 1967 see column 2, line 71 - column 3, line 22	1

* Special categories of cited documents: [15]
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IV. CERTIFICATION

Date of the Actual Completion of the International Search [1]	Date of Mailing of this International Search Report [1]
29th October 1984	15 NOV. 1984
International Searching Authority [1]	Signature of Authorized Officer [20]
EUROPEAN PATENT OFFICE	G.L.M. Bruyckenberg

Form PCT/ISA/210 (second sheet) (October 1981)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 84/0132^ (SA 7733)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 09/11/84

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Patent document cited in search report	Publication date	Patent family member(s)	Publicati date
DE-A- 2801684	19/07/79	None	
US-A- 3354380		None	

For more details about this annex :
see Official Journal of the European Patent Office, No. 12/82